WHAT IS CLAIMED IS:

1. A semiconductor device evaluation method comprising the steps of:

(a) for a plurality of insulated gate transistors with different channel lengths, determining an effective channel length Leff, a gate capacitance Cg which is a capacitance between a gate and a substrate, and a fringing capacitance Cf which is a capacitance between said gate and a portion of said substrate not covered with said gate, by electrical measurement and/or calculation;

(b) plotting said gate capacitance Cg and said effective channel length Leff, which have been determined in said step (a), on a graph and extending the same by extrapolation on said graph to determine gate-capacitance-vs.-effective-channel-length characteristics; and

(c) calculating a gradient A of said gate-capacitance-vs.-effective-channel-length characteristics and determining a finished gate length Lg for each of said plurality of insulated gate transistors from the equation, $Lg = (Cg - Cf)/A$.

2. The semiconductor device evaluation method according to claim 1, wherein

said step (a) prepares a design gate length Ld instead of determining said effective channel length Leff by electrical measurement and/or calculation,

said step (b) plots said gate capacitance Cg and said design gate length Ld, which have been determined in said step (a), on a graph and extends the same by extrapolation on said graph to determine gate-capacitance-vs.-design-gate-length instead of determining said gate-capacitance-vs.-effective-channel-length characteristics, and

said step (c) calculates a gradient of said gate-capacitance-vs.-design-gate-length characteristics as said gradient A, instead of calculating the gradient of said gate-capacitance-vs.-effective-channel-length characteristics.

3. The semiconductor device evaluation method according to claim 1, wherein said step (b) carries out said extrapolation of said characteristics by linear approximation.

4. The semiconductor device evaluation method according to claim 1, further comprising the steps of:

(d) determining an intercept B of said gate-capacitance-vs.-effective-channel-length characteristics; and

(e) for said plurality of insulated gate transistors, determining a gate overlap capacitance CGDO which is a capacitance between said gate and a source/drain region covered with said gate, from the equation, $CGDO = B/(2 \cdot W) - Cf$, by using a gate width W of said gate.

5. The semiconductor device evaluation method according to claim 1, further comprising the step of:

(f) for said plurality of insulated gate transistors, determining an effective gate insulating film thickness Toxeff from the equation, $Toxeff = W \cdot \varepsilon ox / A$, by using said gradient A, a gate width W of said gate, and the permittivity εox of a gate insulating film.

6. A computer-readable recording medium for recording a program which is executed by a computer either by itself or in combination with a preinstalled program in said computer, to carry out said semiconductor device evaluation method according to claim 1.

7. A semiconductor device evaluation apparatus comprising:

a calculation section for, for a plurality of insulated gate transistors with different channel lengths, plotting an effective channel length Leff and a gate capacitance Cg which is a capacitance between a gate and a substrate, on a graph and extending the same by extrapolation on said graph to determine gate-capacitance-vs.-effective-channel-length characteristics, and calculating a gradient A of said characteristics;

a first determination section for determining a finished gate length Lg for each of said plurality of insulated gate transistors from the equation, $Lg = (Cg - Cf)/A$, by using a fringing capacitance Cf which is a capacitance between said gate and a portion of said substrate not covered with said gate, said gradient A, and said gate capacitance Cg; and

a control section for controlling said calculation section and said first determination section.

8. The semiconductor device evaluation apparatus according to claim 7, wherein

said calculation section uses a design gate length Ld instead of said effective channel length Leff,

said calculation section plots said gate capacitance Cg and said design gate length Ld on a graph and extends the same by extrapolation on said graph to determine gate-capacitance-vs.-design-gate-length characteristics, instead of determining said gate-capacitance-vs.-effective-channel-length characteristics, and

said calculation section calculates a gradient of said gate-capacitance-vs.-design-gate-length characteristics as said gradient A, instead of calculating the gradient of

said gate-capacitance-vs.-effective-channel-length characteristics.

9. The semiconductor device evaluation apparatus according to claim 7, wherein

said calculation section carries out said extrapolation of said characteristics by linear approximation.

10. The semiconductor device evaluation apparatus according to claim 7, wherein

said calculation section further determines an intercept B of said gate-capacitance-vs.-effective-channel-length characteristics,

said apparatus further comprising:

a second determination section for, for said plurality of insulated gate transistors, determining a gate overlap capacitance CGDO which is a capacitance between said gate and a source/drain region covered with said gate, from the equation, $CGDO = B/(2 \cdot W) - Cf$, by using a gate width W of said gate,

wherein said second determination section is also controlled by said control section.

11. The semiconductor device evaluation apparatus according to claim 7, further comprising:

a third determination section for, for said plurality of insulated gate transistors, determining an effective gate insulating film thickness Toxeff from the equation, $Toxeff = W \cdot \varepsilon ox / A$, by using said gradient A, a gate width W of said gate, and the permittivity εox of a gate insulating film,

wherein said third determination section is also controlled by said control section.

12. A semiconductor device evaluation method comprising the steps of:

(a) while regarding a plurality of insulated gate transistors with different gate length as a plurality of resistive elements with different line widths Lg each using a gate as a resistance, determining said line width Lg for some of said plurality of resistive elements;

(b) for all of said plurality of resistive elements, determining a resistance Rg of said gate and an effective channel length Leff by electrical measurement and/or calculation;

(c) plotting said line width Lg and said effective channel length Leff, which have been determined in said steps (a) and (b), on a graph and extending the same by extrapolation on said graph to determine line-width-vs.-effective-channel-width characteristics; and

(d) for all of said plurality of resistive elements, determining characteristics between said line width Lg and said resistance Rg by using said line-width-vs.-effective-channel-length characteristics.

13. A semiconductor device evaluation method comprising the steps of:

(g) preparing a finished gate length Lg determined by said semiconductor device evaluation method according to claim 1;

(h) for each of said plurality of insulated gate transistors, determining a resistance Rg of a gate by electrical measurement and/or calculation; and

(i) determining characteristics between said finished gate length Lg and said

resistance Rg.

14. A computer-readable recording medium for recording a program which is executed by a computer either by itself or in combination with a preinstalled program in said computer, to carry out said semiconductor device evaluation method according to claim 12.

15. A semiconductor device evaluation apparatus comprising:

a calculation section for, while regarding a plurality of insulated gate transistors with different channel lengths as a plurality of resistive elements with different line widths Lg each using a gate as a resistance, plotting an effective channel length Leff and said line width Lg for some of said plurality of resistive elements on a graph and extending the same by extrapolation on said graph to determine line-width-vs.-effective-channel-length characteristics;

a determination section for, for all of said plurality of resistive elements, determining characteristics between said line width Lg and a resistance Rg of said gate by using said line-width-vs.-effective-channel-length characteristics; and

a control section for controlling said calculation section and said determination section.

16. A semiconductor device evaluation apparatus comprising:

a determination section for determining characteristics between a finished gate length Lg obtained by said semiconductor device evaluation method according to claim 1, and a resistance Rg of a gate for each of said plurality of insulated gate transistors; and

a control section for controlling said determination section.

17. A semiconductor device manufacturing control method comprising:

a judgment step for judging whether said finished gate length Lg of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method according to claim 1, meets required standard,

wherein a result of judgment in said judgment step is utilized for reappraisal of manufacturing conditions of semiconductor devices.

18. A semiconductor device manufacturing method comprising

a judgment step for judging whether said finished gate length Lg of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method according to claim 1, meets required standards,

wherein a result of judgment in said judgment step is utilized for rejection of nonconforming products.

19. A semiconductor device manufacturing control method comprising:

a judgment step for judging whether said resistance Rg of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method according to claim 12, meets required standards,

wherein a result of judgment in said judgment step is utilized for reappraisal of manufacturing conditions of semiconductor devices.

20. A semiconductor device manufacturing method comprising:

a judgment step for judging whether said resistance Rg of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method

according to claim 12, meets required standards,

wherein a result of judgment in said judgment step is utilized for rejection of nonconforming products.